10072870-021202

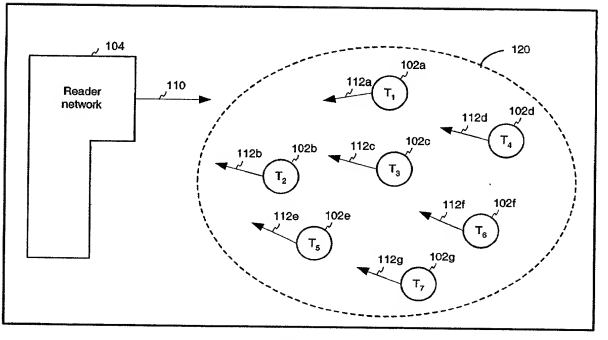

FIG. 1

20210208.0421201

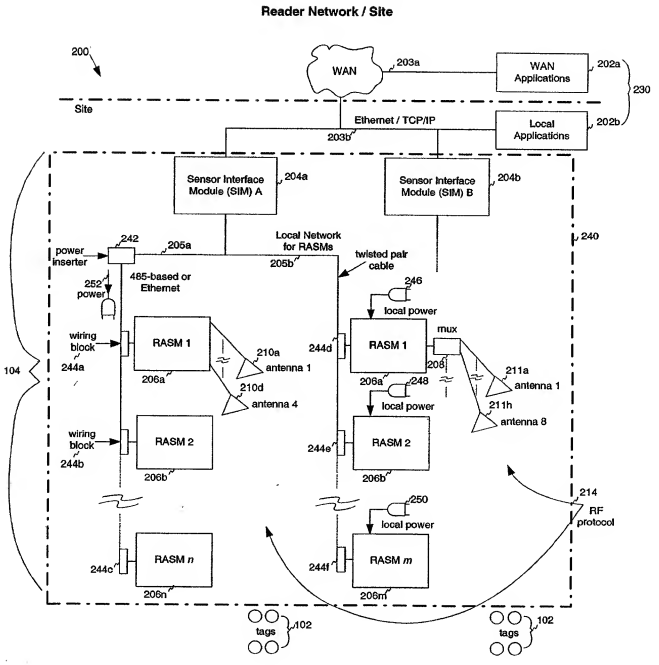

FIG. 2

10072370 "022202

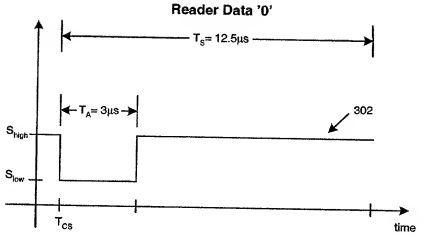

FIG. 3

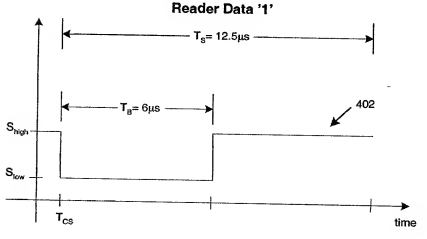

FIG. 4

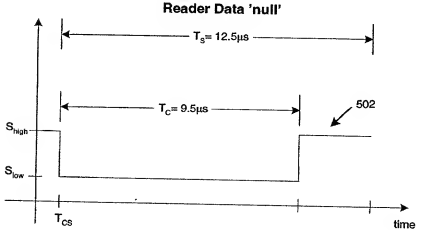

FIG. 5

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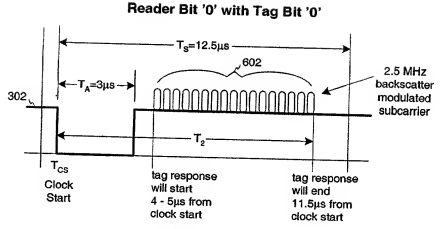

FIG. 6

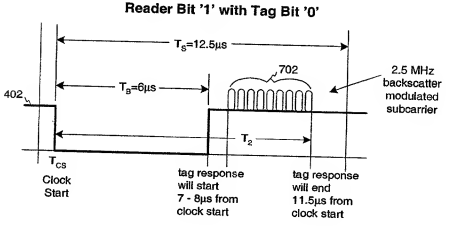

FIG. 7

Reader Bit '0' with Tag Bit '1'

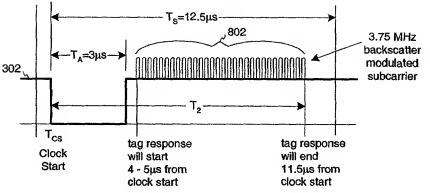

FIG. 8

Reader Bit '1' with Tag Bit '1'

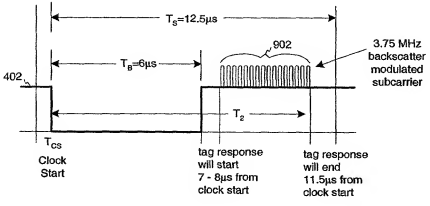

FIG. 9

Patent-8,537,007

10/22/2002 20:20:20

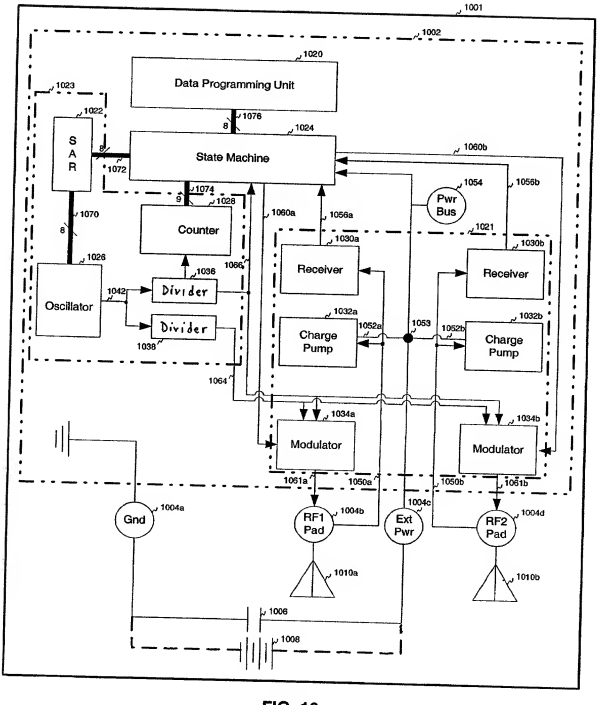

FIG. 10

PENDING-DESIGN

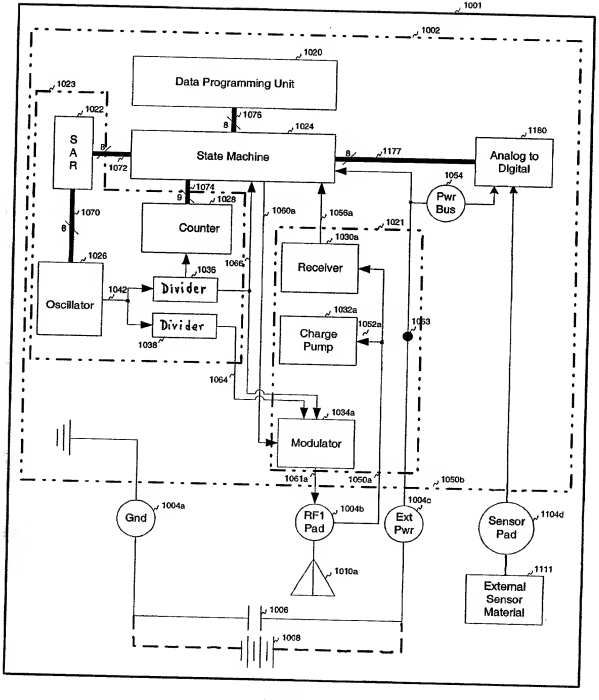

FIG. 11

10072870-021202

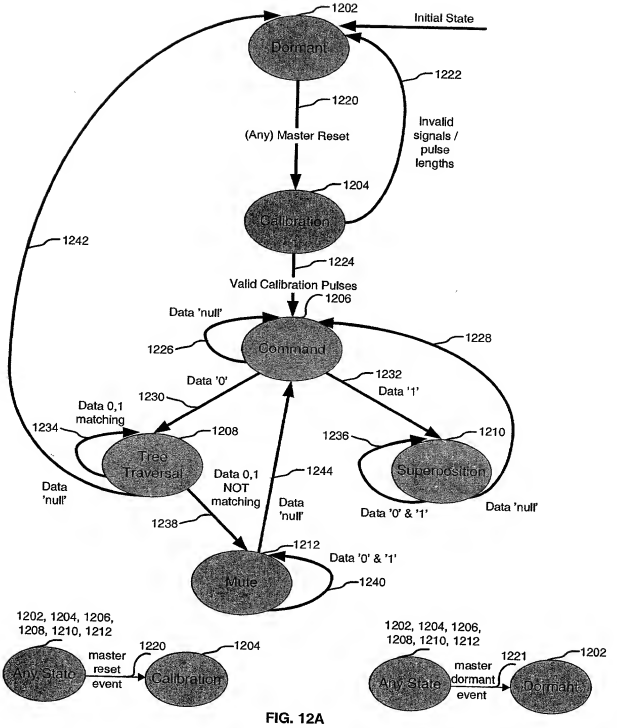

FIG. 12A

0201-20b.vsd/8

0201-20b.vsd/9

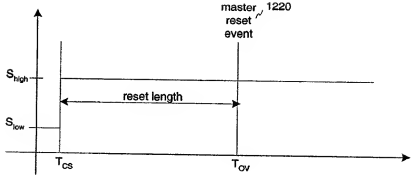

FIG. 12B

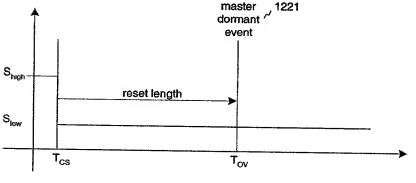

FIG. 12C

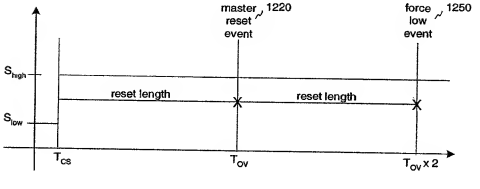

FIG. 12D

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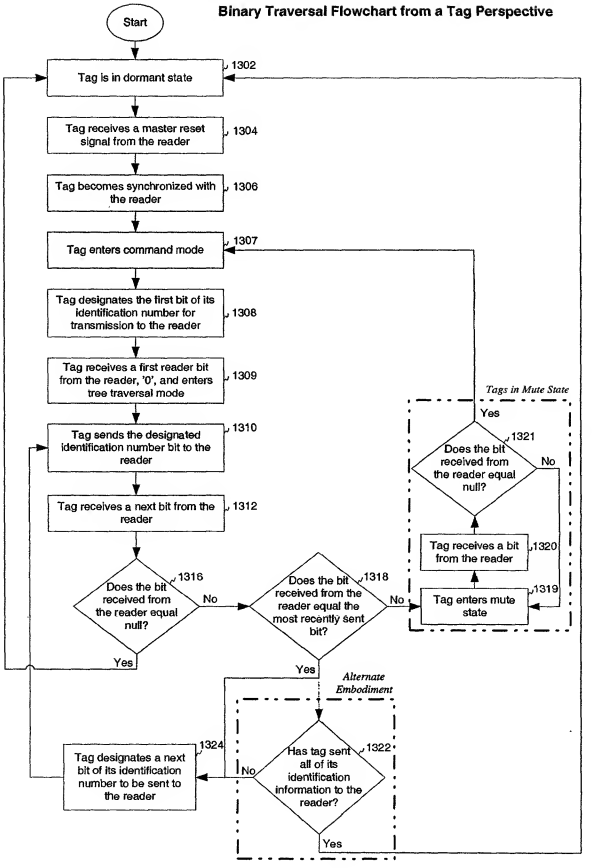

FIG.13

0201-20b.vsd/10

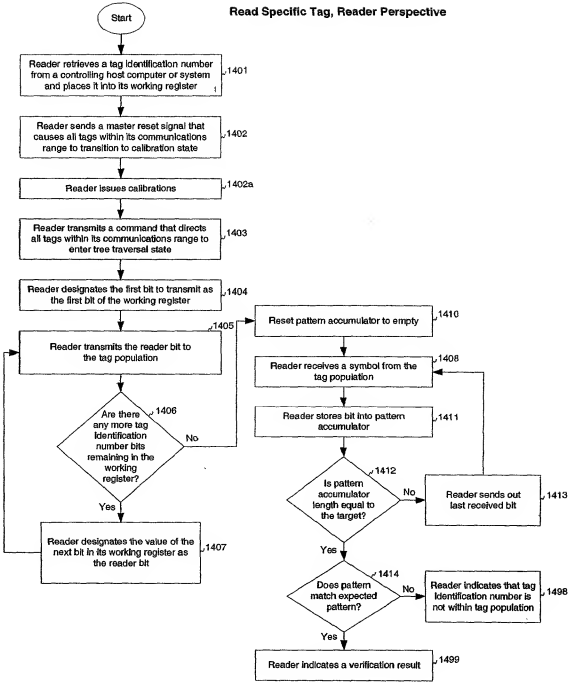
Read Specific Tag, Reader Perspective
Start
Reader retrieves a tag identification number from a controlling host computer or system and places it into its working register
1401
Reader sends a master reset signal that causes all tags within its communications range to transition to calibration state
1402
Reader issues calibrations
1402a
Reader transmits a command that directs all tags within its communications range to enter tree traversal state
1403
Reader designates the first bit to transmit as the first bit of the working register
1404
1405
Reader transmits the reader bit to the tag population
Are there any more tag identification number bits remaining in the working register?
1406
No
Yes
Reader designates the value of the next bit in its working register as the reader bit
1407
Reset pattern accumulator to empty
1410
Reader receives a symbol from the tag population
1408
Reader stores bit into pattern accumulator
1411
Is pattern accumulator length equal to the target?
1412
No
Reader sends out last received bit
1413
Yes
Does pattern match expected pattern?
1414
No
Reader indicates that tag identification number is not within tag population
1498
Yes
Reader indicates a verification result
1499

FIG. 14A

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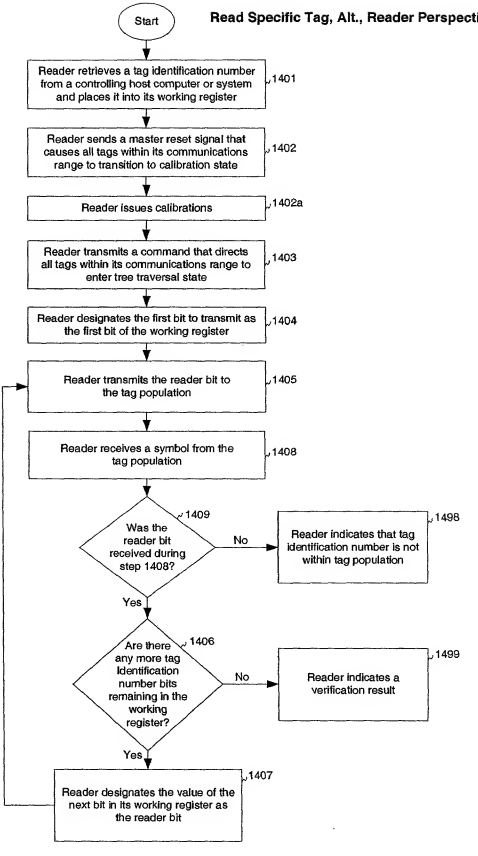

FIG. 14B

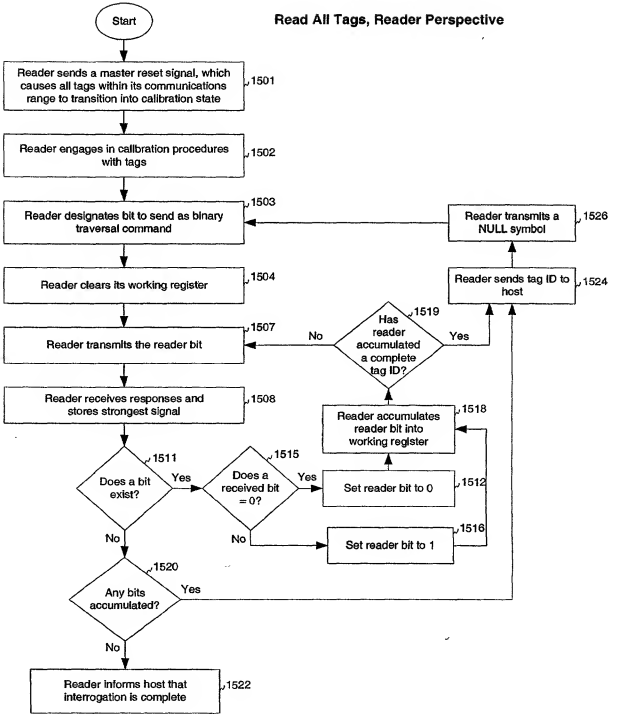
Read All Tags, Reader Perspective
Start
Reader sends a master reset signal, which causes all tags within its communications range to transition into calibration state
1501
Reader engages in calibration procedures with tags
1502
Reader designates bit to send as binary traversal command
1503
Reader clears its working register
1504
Reader transmits the reader bit
1507
Reader receives responses and stores strongest signal
1508
Does a bit exist?
1511
Yes
Does a received bit = 0?
1515
Yes
Set reader bit to 0
1512
No
Set reader bit to 1
1516
Reader accumulates reader bit into working register
1518
Has reader accumulated a complete tag ID?
1519
No
Yes
Reader transmits a NULL symbol
1526
Reader sends tag ID to host
1524
Any bits accumulated?
1520
Yes
No
Reader informs host that interrogation is complete
1522

FIG. 15A

20120102007

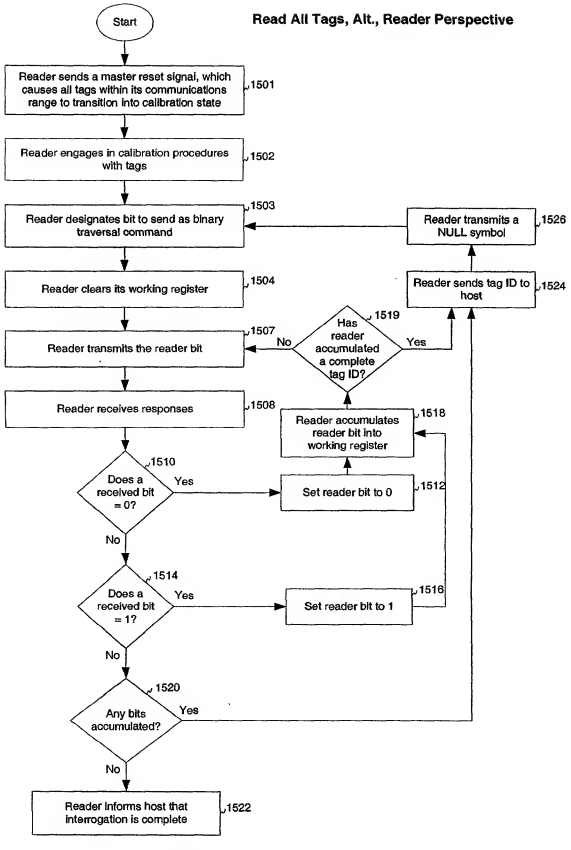

FIG. 15B

10072870.021202

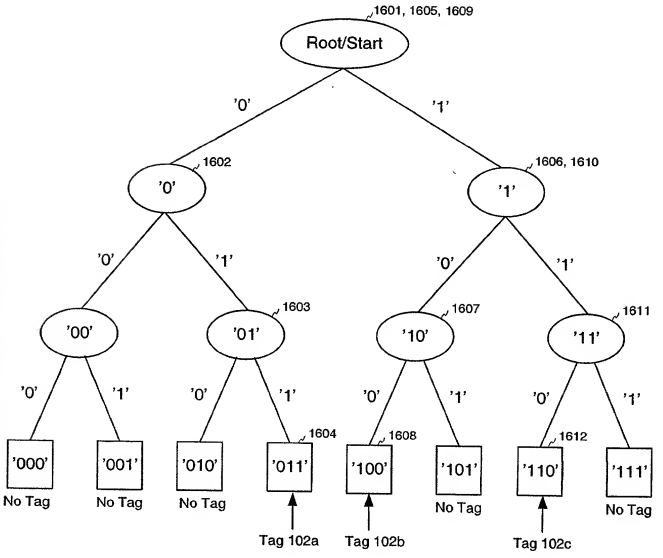

FIG. 16

10025/20.02202

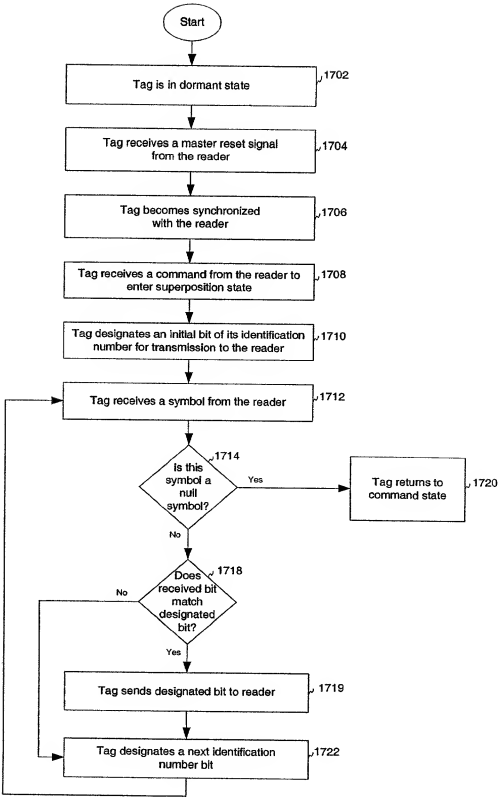

FIG. 17A

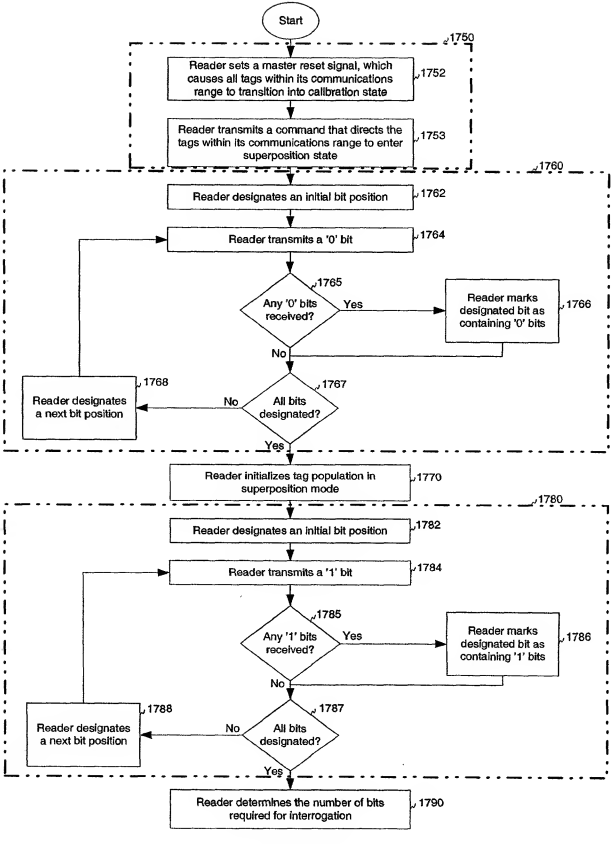

FIG. 17B

0201-20b.vsd/17

10072870.021202

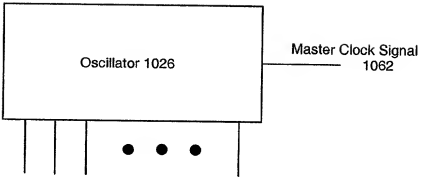

FIG. 18

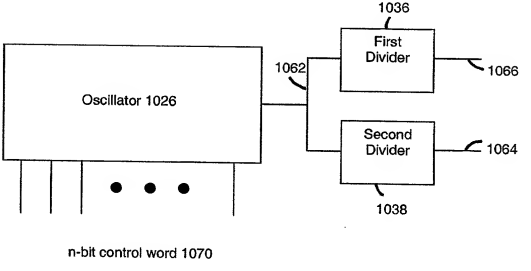

FIG. 19

20120702/20120702

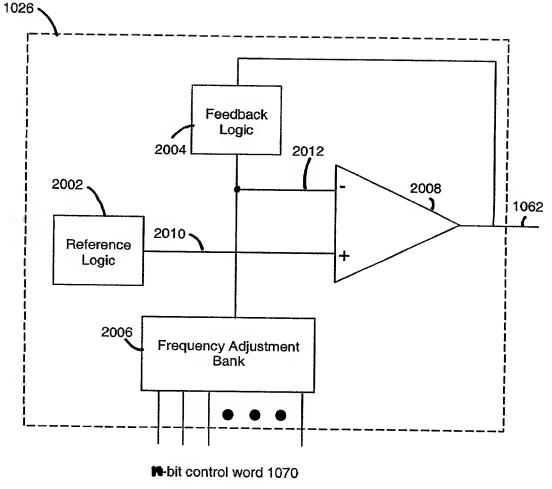

FIG. 20

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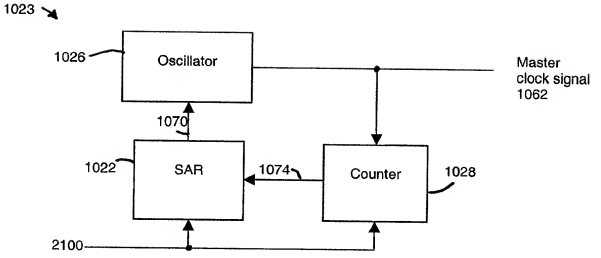

FIG. 21A

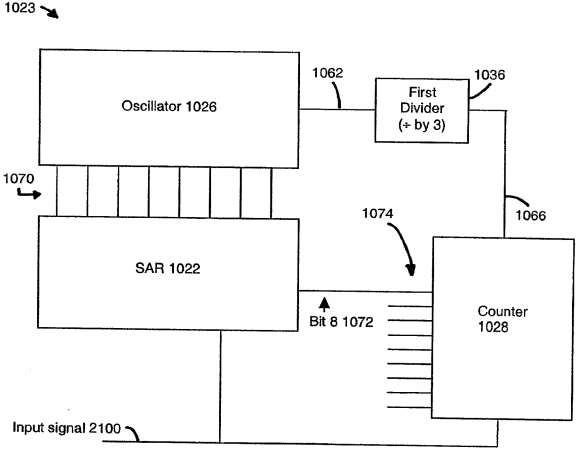

FIG. 21B

1007280.021202

Conceptual implementation of SAR calibration

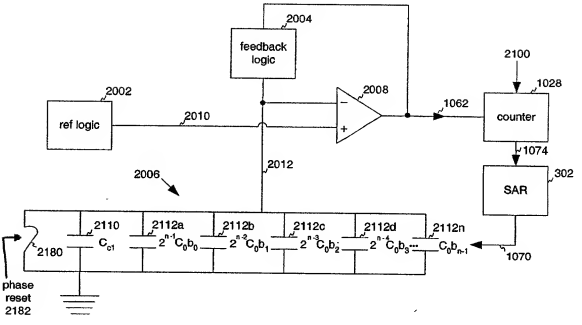

FIG. 21C

Physical implementation of adjustable capacitor bank

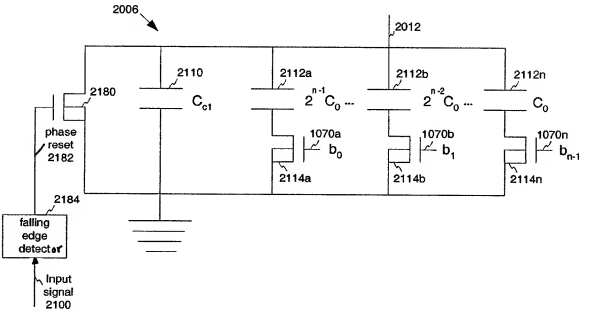

FIG. 21D

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20212020-07-02 12:07:01

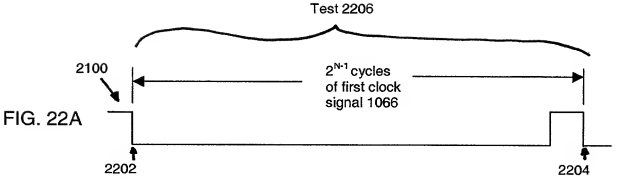

FIG. 22A

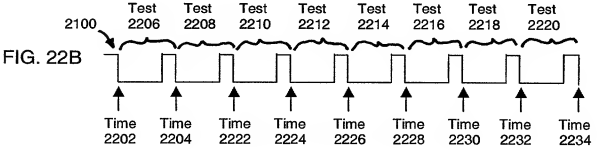

FIG. 22B

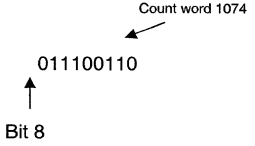

FIG. 23A

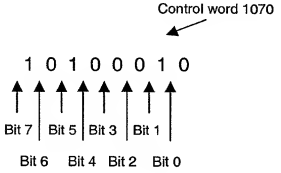

FIG. 23B

0201-20b.vsd/23

20120702.0822.007

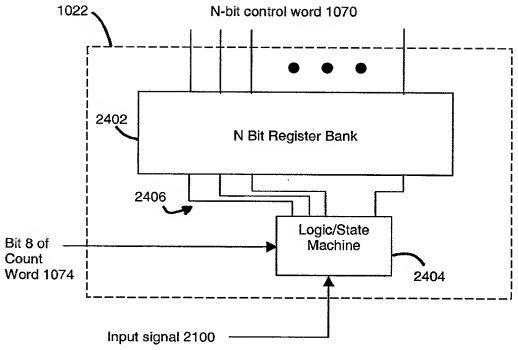

FIG. 24

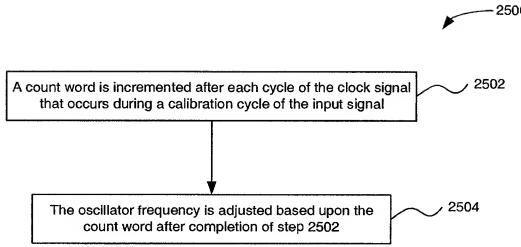

FIG. 25A

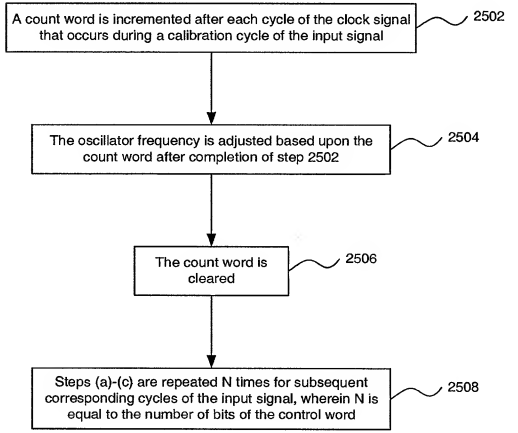

FIG. 25B

1007287.021202

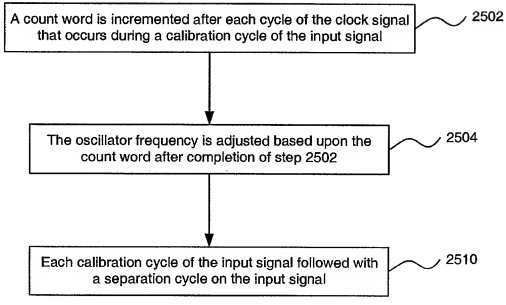

FIG. 25C

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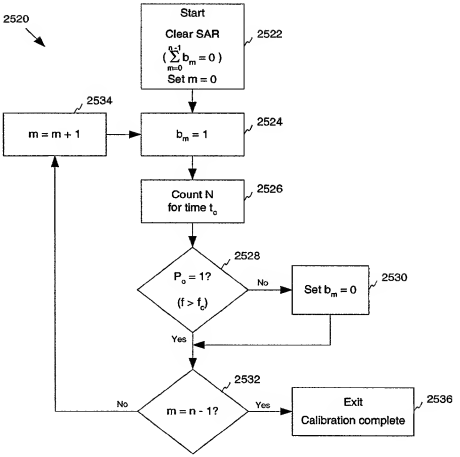

FIG. 25D

100720.0212202

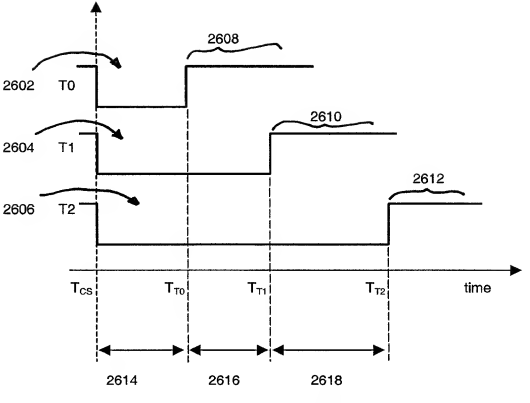

FIG. 26A

Data Symbol Timing Chart

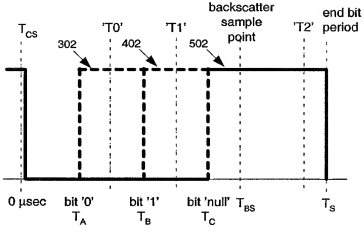

FIG. 26B

10072870.021202

20212020-0021202 1007287.0

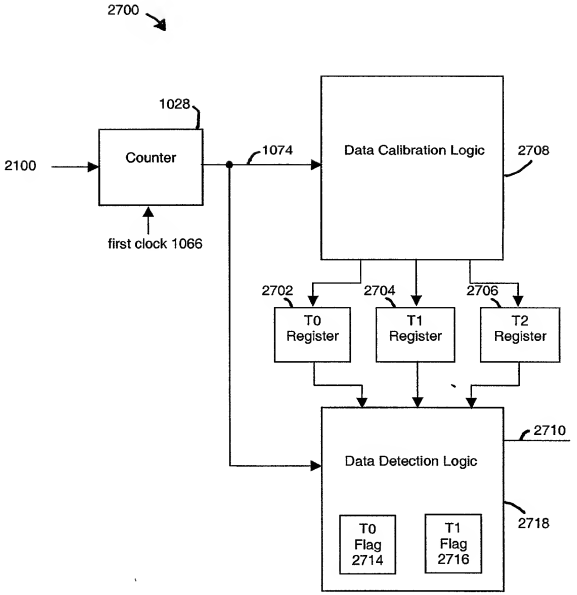

FIG. 27

20120213.0837/0012202.1

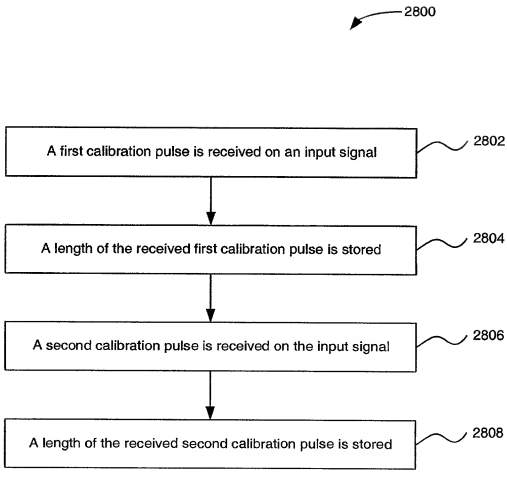

FIG. 28A

10072570.021202

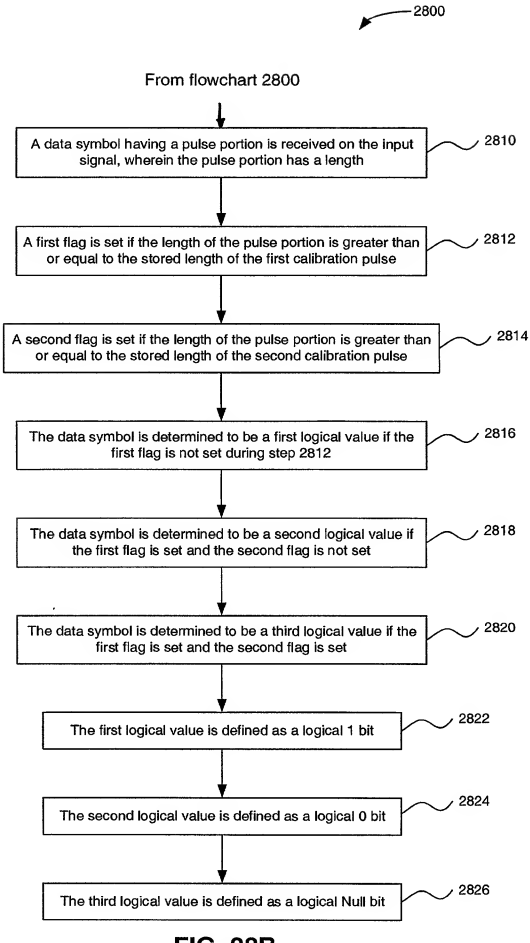

FIG. 28B

0201-20b.vsd/32

10/28/0 02:12:02

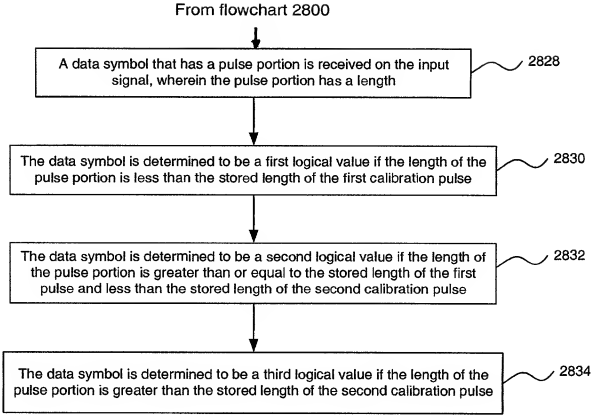

FIG. 28C

10076670-021202

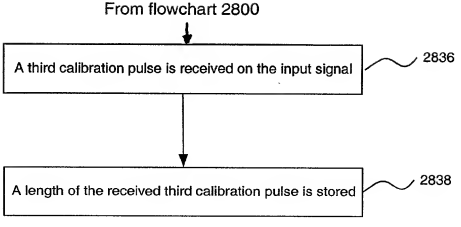

FIG. 28D

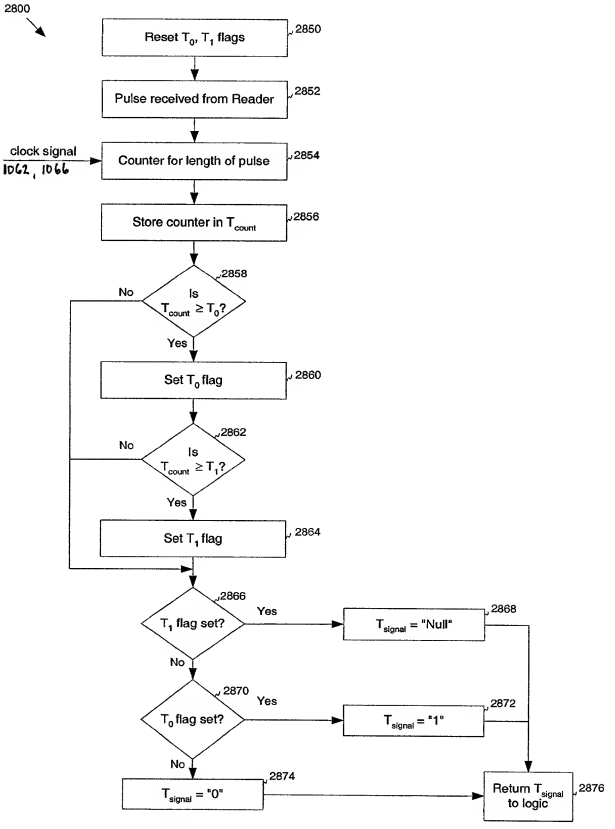
2800
Reset T_0, T_1 flags
2850
Pulse received from Reader
2852
clock signal
1062, 1066
Counter for length of pulse
2854
Store counter in T_{count}
2856
Is $T_{count} \geq T_0$?
2858
No
Yes
Set T_0 flag
2860
Is $T_{count} \geq T_1$?
2862
No
Yes
Set T_1 flag
2864
T_1 flag set?
2866
Yes
T_{signal} = "Null"
2868
No
T_0 flag set?
2870
Yes
T_{signal} = "1"
2872
No
T_{signal} = "0"
2874
Return T_{signal} to logic
2876

FIG. 28E

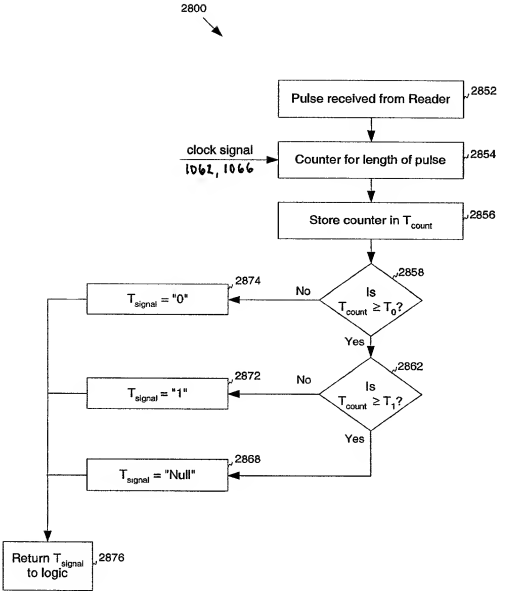
2800
Pulse received from Reader
2852
clock signal
1062, 1066
Counter for length of pulse
2854
Store counter in T_{count}
2856
Is $T_{count} \geq T_0$?
2858
No
T_{signal} = "0"
2874
Yes
Is $T_{count} \geq T_1$?
2862
No
T_{signal} = "1"
2872
Yes
T_{signal} = "Null"
2868
Return T_{signal} to logic
2876

FIG. 28F

20120720.0212202

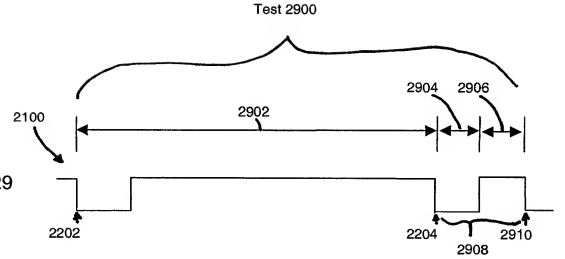

FIG. 29

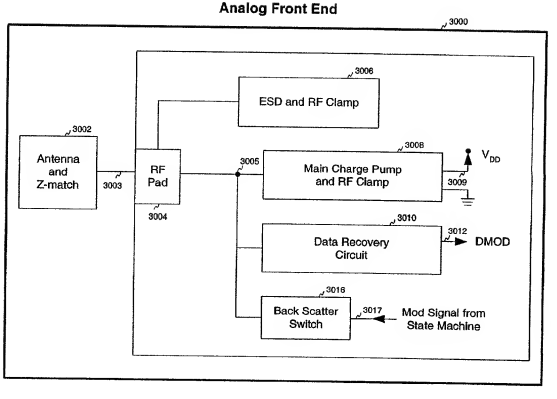
Analog Front End
3000
3006
ESD and RF Clamp
3002
Antenna and Z-match
3003
RF Pad
3004
3005
3008
Main Charge Pump and RF Clamp
3009
V_{DD}
3010
Data Recovery Circuit
3012
DMOD
3016
Back Scatter Switch
3017
Mod Signal from State Machine

FIG. 30

20210107287

FIG. 31

2012-02-29

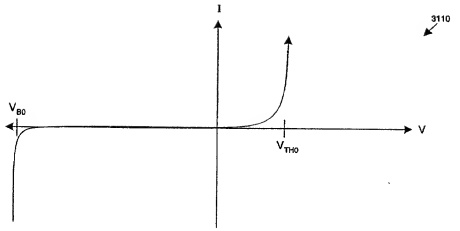

FIG. 32A

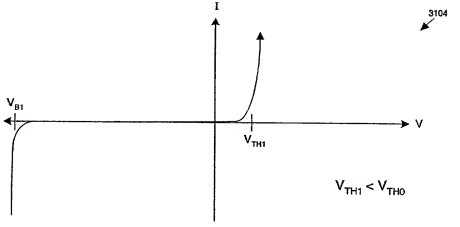

FIG. 32B

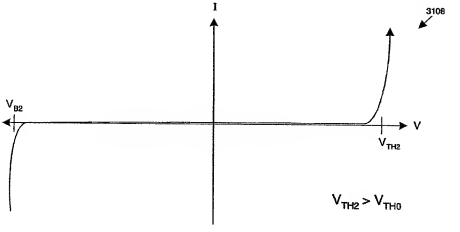

FIG. 32C

10/2670-021202

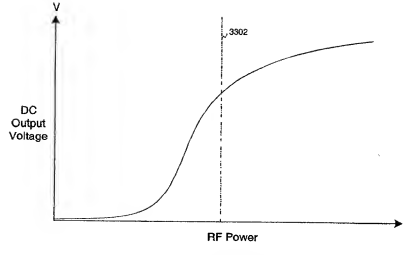

FIG. 33A

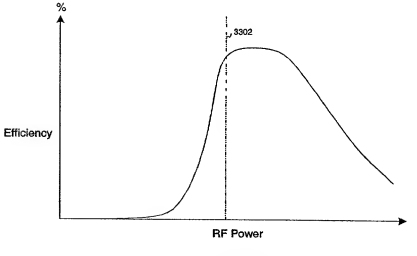

FIG 33B

20210210.0282007

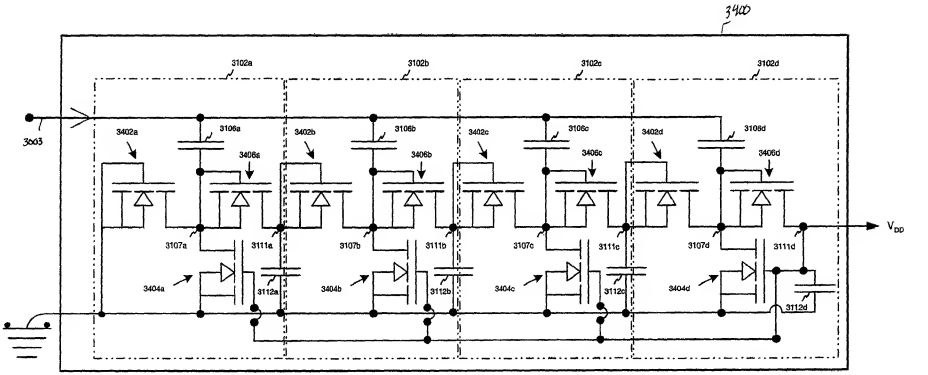

FIG. 34A

20210201.0822001

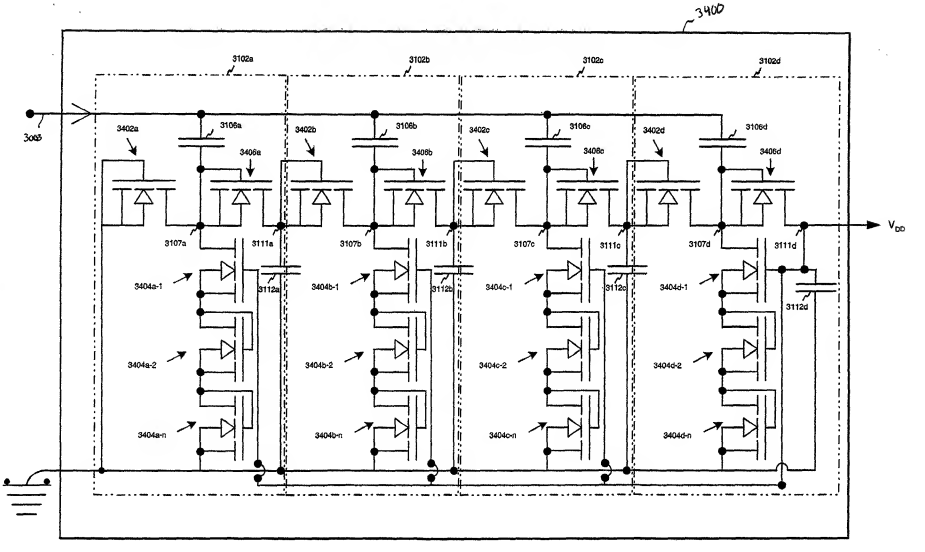

FIG. 34B

Printed: 07/25/2007

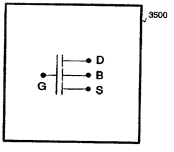

FIG. 35A

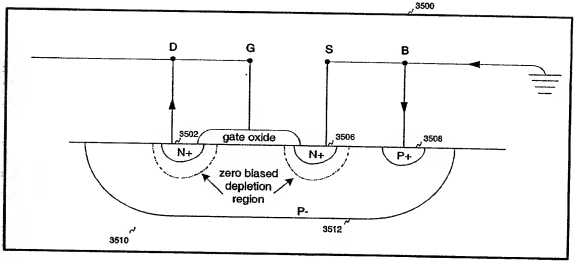

FIG. 35B

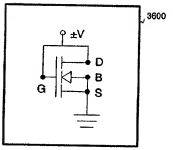

FIG. 36A

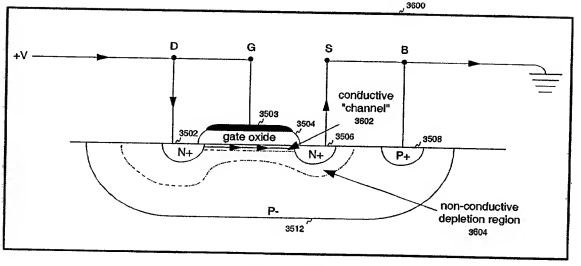

FIG. 36B

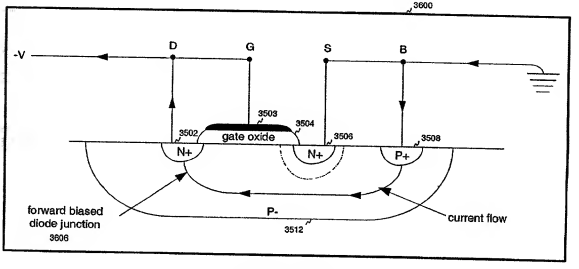

FIG. 36C

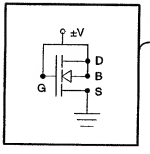

FIG. 37A

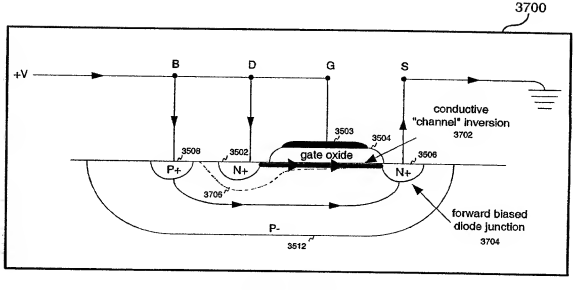

FIG. 37B

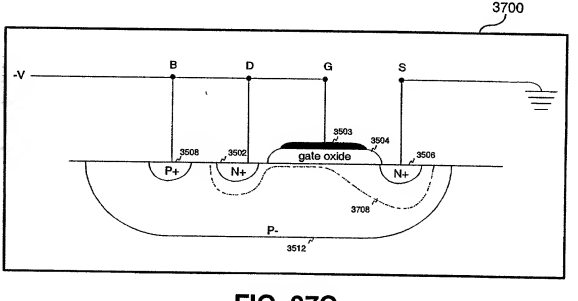

FIG. 37C

2012220070.2012/08/27

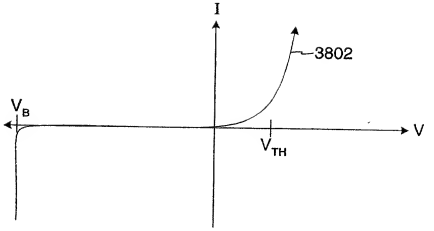

FIG. 38A

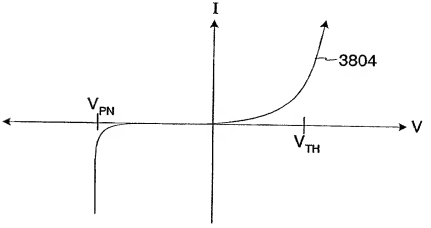

FIG. 38B

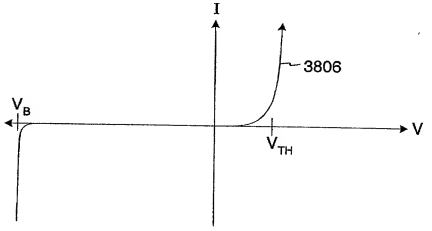

FIG. 38C

20120270 • 01/26/2012

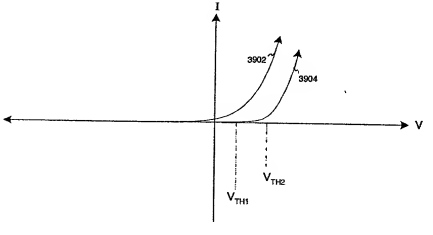

FIG. 39

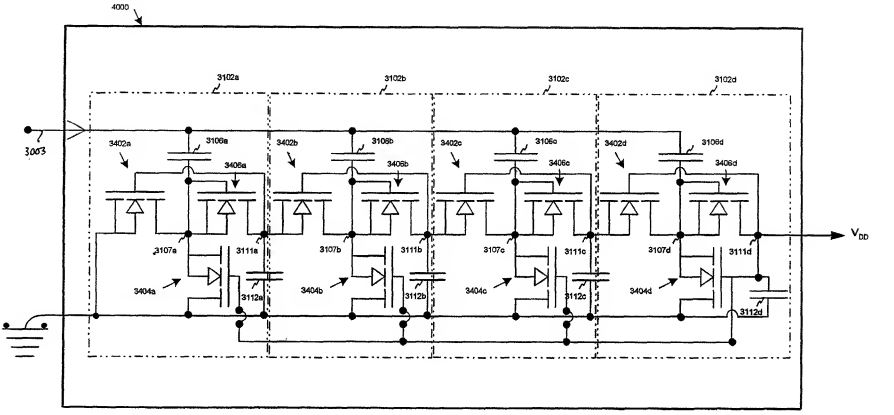
4000
3102a
3102b
3102c
3102d
3003
3402a
3106a
3406a
3107a
3111a
3404a
3112a
3402b
3106b
3406b
3107b
3111b
3404b
3112b
3402c
3106c
3406c
3107c
3111c
3404c
3112c
3402d
3106d
3406d
3107d
3111d
3404d
3112d
V_{DD}

FIG. 40A

20210210.0728700

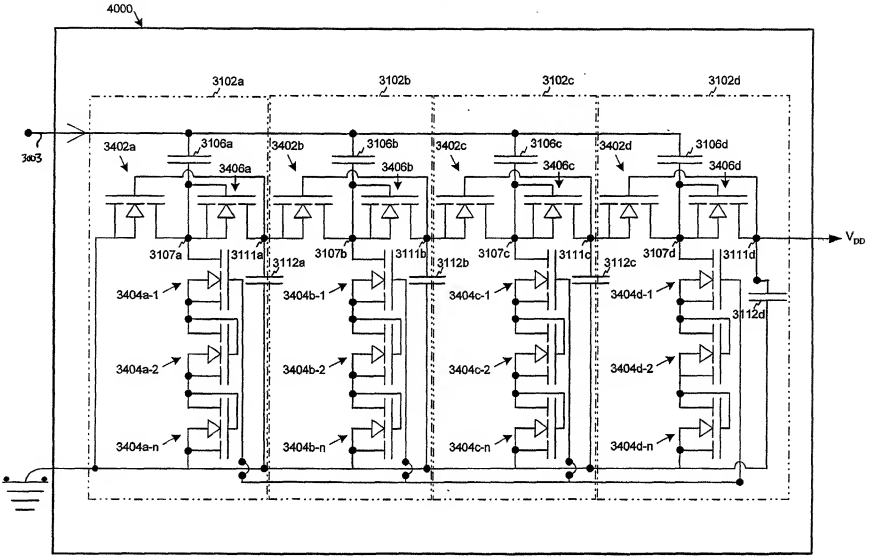

FIG. 40B

US 2007/0247202 A1

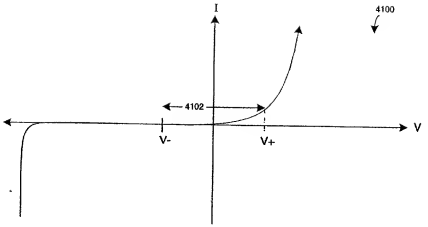

FIG. 41A

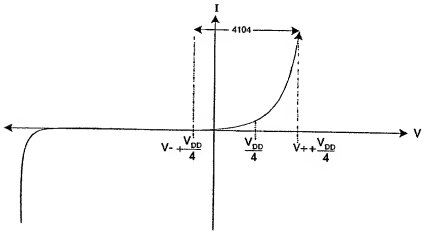

FIG. 41B

10/728,702 - 02/12/2008

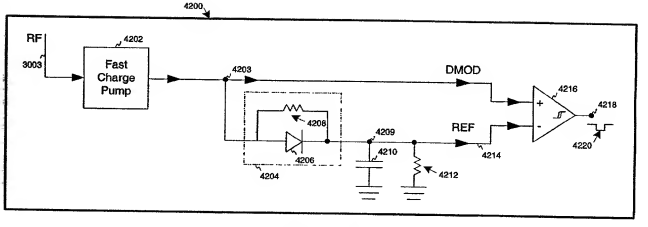

FIG. 42

JP0023970.021202

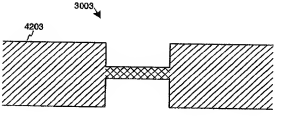

FIG. 43A

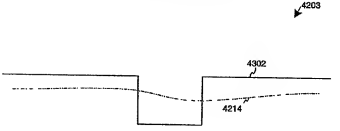

FIG. 43B

20210204-US-62/970,402

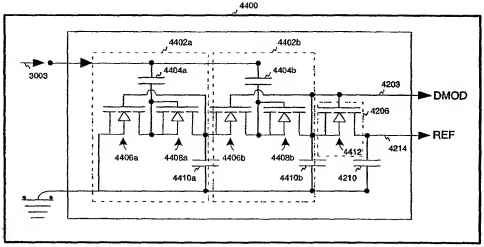

FIG. 44

10072870-021202

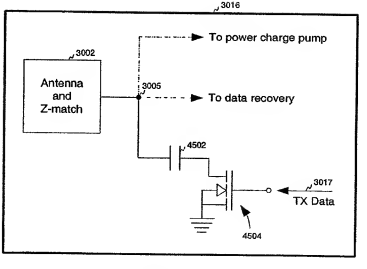

FIG. 45